FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
	INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	03-I-712 (850063.603RI)	10/631,323
		APPLICANTS: Vito Fabbrizio et al.	
		FILING DATE: July 31, 2003	GROUP ART UNIT: ~~2122~~ 2129

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,956,564	09/11/90	Holler et al.	307	201	
	AB	4,961,002	10/02/90	Tam et al.	307	201	
	AC	4,988,891	01/29/91	Mashiko	307	201	
	AD	5,004,932	04/02/91	Nejime	307	201	
	AE	5,021,693	06/04/91	Shima	307	494	
	AF	5,021,988	06/04/91	Mashiko	364	807	
	AG	5,053,638	10/01/91	Furutani et al.	307	201	
	AH	5,056,037	10/08/91	Eberhardt	364	513	
	AI	5,101,361	03/31/92	Eberhardt	395	24	
	AJ	5,146,602	09/08/92	Holler et al.	395	23	
	AK	5,150,450	09/22/92	Swenson et al.	395	23	
	AL	5,155,377	10/13/92	Castro	307	201	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AM	0 349 007 B1	12/20/95	EP		

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AN	Benson, R. et al., "UV-Activated Conductances Allow for Multiple Time Scale Learning," *IEEE Trans. on Neural Networks 4*(3):434-440, May 1993.
	AO	Boser, B. et al., "An Analog Neural Network Processor with Programmable Topology," *IEEE J. of Solid State Circuits 26*(12):2017-2025, December 1991.
	AP	Chandraksan, A. et al., "Low-Power CMOS Digital Design," *IEEE J. of Solid-State Circuits 27*(4):473-484, April 1992.
	AQ	Cosatto, E. et al., "NET31K High Speed Image understanding System," in *Proc. Fourth Intl. Conf. on Microelectronics for Neural Networks and Fuzzy Systems*, IEEE Computer Society Press, Los Alamitos, CA, 1994, pp. 413-421.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BB/

FORM PTO-1449 (REV.7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
	03-I-712 (850063.603RI)	10/631,323
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS: Vito Fabbrizio et al.	
	FILING DATE: July 31, 2003	GROUP ART UNIT: ~~2122~~ 2129

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	BA	5,155,802	10/13/92	Mueller et al.	395	24	
	BB	5,187,680	02/16/93	Engeler	364	807	
	BC	5,202,956	04/13/93	Mashiko	395	24	
	BD	5,248,956	09/28/93	Himes et al.	338	334	
	BE	5,256,911	10/26/93	Holler et al.	307	201	
	BF	5,258,657	11/02/93	Shibata et al.	307	201	
	BG	5,268,320	12/07/93	Holler et al.	437	43	
	BH	5,274,746	12/28/93	Mashiko	395	27	
	BI	5,298,796	03/29/94	Tawel	307	201	
	BJ	5,299,286	03/29/94	Imondi et al.	395	27	
	BK	5,305,250	04/19/94	Salam et al.	364	807	
	BL	5,336,937	08/09/94	Sridhar at el.	307	201	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	BM					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	BN		Degrauwe, M. et al., "A Micropower CMOS-Instrumentation Amplifier," *IEEE J. of Solid-State Circuits 20*(3):805-807, June 1985.
	BN		Fabbrizio, V. et al., "Low Power, Low Voltage Conductance-Mode CMOS Analog Neuron," in *Proc. of MicroNeuro '96*, pp. 111-115, February 1996.
	BP		Graf, H. et al., "A CMOS Associative Memory chip," in *Proc. IEEE First Intl. Conf. neural Newtworks, M. Caudill and C. Butler (ed.)*, SOS Printing, San Diego, CA 1987, pp. III-461 – III-468.
	BQ		Graf, H. et al., "A Reconfigurable CMOS Neural Network," *IEEE ISSCC*, pp. 144-145, February 1990.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BB/

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 03-I-712 (850063.603RI)	APPLICATION NO. 10/631,323
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANTS Vito Fabbrizio et al.	
		FILING DATE July 31, 2003	GROUP ART UNIT ~~2122~~ 2129

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	CA	5,343,555	08/30/94	Yayla et al.	395	24	
	CB	5,396,581	03/07/95	Mashiko	395	24	
	CC	5,422,982	06/06/95	Pernisz	395	24	
	CD	5,444,821	08/22/95	Li et al.	395	24	
	CE	5,475,794	12/12/95	Mashiko	395	24	
	CF	5,509,105	04/16/96	Roenker et al.	395	24	
	CG	5,615,305	03/25/97	Nunally	395	24	
	CH	5,704,014	12/30/97	Marotta et al.	395	24	
	CI	6,032,040	02/29/00	Fabbrizio et al.	706	15	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	CJ					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	CK	Guardiani, C. et al., "Applying a Submicron Mismatch Model to Practical IC Design," in *Proc. of the CICC*, pp. 13.3.1-13.3.1, 1994.
	CL	Holler, M. et al., "An Electrically Trainable Artificial Neural Network (ETANN)with 10240 'Floating Gate' Synapses," in *Proc. IJCNN*, pp. 2.191-2.196, June 1989.
	CM	Hollis, P. et al., "Artificial Neural Networks Using MOS Analog Multipliers," *IEEE J. of Solid-State Circuits 25*(3):849-855, June 1990.
	CN	Jain, J. et al., "Displacement Measurement and Its Application in Interframe Image Coding," *IEEE Trans. on Communications COM-29*(12):1799-1808, December 1981.
	CO	König, A. et al., "Massively Parallel VLSI-Implementation of a Dedicated Neural Network for Anomaly Detection in Automated Visual Quality Control," in *Proc. of the 4th Intl. Conf of Microelectronics for Neural Networks and Fuzzy Systems*, Turin, Italy, September 26-28, 1994, pp. 354-364.
	CP	Kovács-V, Z. et al., "Massively-Parallel Handwritten Character Recognition Based on the Distance Transform," *Pattern Recognition 28*(3):293-301, 1995.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BB/

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 03-I-712 (850063.603RI)	APPLICATION NO. 10/631,323
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANTS Vito Fabbrizio et al.	
		FILING DATE July 31, 2003	GROUP ART UNIT ~~2122~~ 2129

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	~~CLASS~~	SUBCLASS	FILING DATE IF APPROPRIATE
	DA						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	DB					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	DC	Kramer, A. et al., "EEPROM Device as a Reconfigurable Analog Element For Neural Networks," *IEDM Tech. Digest*, pp. 10.3.1-10.3.4, December 1989.
	DD	Kramer, A. et al., "Ultra-Low-Power Analog Associative Memory Core Using Flash-EEPROM-Based Programmable Capacitors," in *Proc. of the 1995 Intl. Symposium on Low Power Design*, Assoc. for Computing Machinery, Dana Point, CA, 1995, pp. 203-208.
	DE	Kramer, A. et al., "Flash-Based Programmable Nonlinear Capacitor for Switched-Capacitor Implementations of Neural networks," *IEDM Tech. Dig.*, pp. 17.6.1-17.6.4, December 1994.
	DF	Lazzaro, J. et al., "Systems Technologies for Silicon Auditory Models," *IEEE Micro 14*(3):7-15, June 1994.
	DG	Lee, B. et al., "Analog Floating-Gate Synapses for General-Purpose VLSI Neural Computation," *IEEE. Trans. on Circuits and Systems 38*(6):654-658, June 1991.
	DH	Mizugaki, Y .et al., "Implementation of New Superconducting Neural Circuits using Coupled SQUIDs," *IEEE Transcriptions on Applied Superconductivity 4*(1):1-8, March 1994.
	DI	Sage, J. et al., "An Artificial Neural Network Integrated Circuit Based on MNOS/CCD Principles," in *Proc. Conf. Neural Networks for Computing, J.S. Denker (ed.)*, Amer. Inst. of Physics, Snowbird, UT, 1986, pp. 381-385.
	DJ	Satyanarayana, S. et al., "A Reconfigurable VLSI Neural Network," *IEEE J. Solid-State Circuits 27*(1):67-81, January 1992.
	DK	Seevinck, E. et al., "A Versatile CMOS Linear Transconductor/Square-Law Function Circuit," *IEEE J. Solid-State Circuits SC-22*(3):366-377, June 1987.
	DL	Sin, C-K. et al., "EEPROM as an Analog Storage Device, with Particular Applications in Neural Networks," *IEEE Trans. on Electron Devices 39*(6):1410-1419, June 1992.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BB/

FORM PTO-1449 (REV.7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 03-I-712 (850063.603RI)	APPLICATION NO. 10/631,323
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Vito Fabbrizio et al.	
	FILING DATE July 31, 2003	GROUP ART UNIT ~~2122~~ 2129

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	EA						
	EB						
	EC						
	ED						
	EE						
	EF						
	EG						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	EH					
	EI					
	EJ					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	EK		Sze, S., *Physics of Semiconductor Devices*, 2 ed., Wiley, 1981, p. 403.
	EL		Tomasini, S. et al., "B/W Adaptive Image Grabber with Analog Motion Vector Estimator at 0.3GOPS," *ISSCC Dig. of Tech. Papers*, pp. 94-95, 425, 1996.
	EM		Tsukano, K. et al., "A New CMOS Neuron Circuit based on a Cross-Coupled Current Comparator Structure," *IEICE Trans. on Fundamentals of Electronics, Comm. and Computer Sciences E75-A*(7):937-943, July 1992.
	EN		White, M. et al., "Electrically Modifiable Nonvolatile Synapses for Neural Networks," *IEEE Intl. Symposium on Circuits and Systems 2*:1213-1216, May 1989.

EXAMINER /Benjamin Buss/	DATE CONSIDERED 12/11/2009

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BB/